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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/051,483	**Applicant(s)** JOO ET AL.
	Examiner Jason M. Perilla	**Art Unit** 2638

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,20-31 and 40-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,20,21,24-26,40-45,48,51,57 and 58* is/are rejected.

7)☒ Claim(s) *2,3,5-11,22,23,27-31,46,47,49,50,52-56 and 59-65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11, 20-31, and 40-65 are pending in the instant application.

Response to Arguments/Amendments

2. In view of the amendments to the claims and the remarks filed August 29, 2005, the claim objections and claim rejections under 35 U.S.C. §112, first and second paragraphs, have been withdrawn.

3. New prior art rejections are set forth below.

Claim Objections

4. Claims 41, and 63-65 are objected to because of the following informalities:

Regarding claim 41, in line 2, the acronym "DDR SDRAM" must be defined in the claim.

Regarding claim 63, in line 4, "defining a group" should be replaced by –defining a respective group--, in line 7, "the data signals, the output delay" should be replaced by –each data signal, the output delay of any one data signal--, in line 9, "the data signals in the associated group" should be replaced by –the corresponding data signals in its associated group--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4, 20, 21, 24, 25, 44, 45, 48, 51, 57, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al (US 6484268; hereafter "Tamura" – previously cited).

Regarding claim 1, Tamura discloses a clock synchronization circuit adapted to receive an input clock signal (fig. 11, "clk") and adapted to receive current data signals (fig. 11, outputs of latches 541-543) and respective future data signals (fig. 11, "DD1-DDn"), the clock synchronization circuit operable to generate a phase shifted clock signal (fig. 1, refs. "clk1-clkn") in response to the input clock signal with the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and respective future data signals. The clock synchronization circuit illustrated in figure 11 of Tamura is utilized to overcome timing differences between the received data signals DD1-DDn (col. 1, lines 45-55). To accomplish this, the timing adjustment circuits (fig. 11, refs. 531-533) each take as input a data signal (DD1, DD2, . . . DDn) as well as the system input clock ("clk") (col. 18, lines 10-20). The input clock is utilized to generate a phase shifted clock signal (i.e. "clk1") respective to each data input signal (i.e. "DD1") based upon current and future data signals DD1 (col. 18, lines 40-63). Figure 14 of Tamura illustrates the timing adjustment circuits (fig. 11, refs. 531-533) in detail. The timing adjustment circuits are comprised of a phase comparator (fig. 14, ref. 5301) and two delay lines (fig. 14, refs. 5302 and 5303) which are adjusted according to the output of the phase comparator. The timing adjustment circuit takes as input one of the data signals "DD1", the input clock signal "clk", and a 180 degree phase shifted version of the "clk" signal "clk'" (col. 19, lines 40-50). The

current data signal of Tamura is the present output of the data latch (fig. 11, ref. 541; fig. 14, ref. 540(541)). The future data signal is the input to the data latch "DD1". Tamura does not explicitly disclose that the current and future data signals are directly compared to phase shift the input clock signal. However, in the iterative clock synchronization circuit of Tamura, the phase shifting of the input clock signal is related to both the current and future data signals. It is obvious to one having skill in the art that a "first data signal" was utilized to update the delay in the delay chains 5302 and 5303 of figure 14 via the phase comparator 5301. Subsequently, after the first data signal was latched as the future data signal (output of 540(541)), a current data signal is compared with a clock signal from the delay circuit 5303 delayed *according to the "first data signal" or the present future data signal.* Hence, using the phase comparator, the current data signal is compared by with a clock signal that is representative of the future data signal, and the phase shifted clock signal clk1 is generated according to the comparison via delay line 5302. Therefore, although Tamura does not explicitly disclose the comparison of the current and future data signals directly, as broadly as claimed, it is inherent, implied, or at least obvious that the phase shifted clock signal has a phase shift which is *a function* of the current and future data signals.

Regarding claim 4, Tamura discloses the limitations of claim 1 as applied above. Further, Tamura discloses that the phase shift of the phase shifted clock signal comprises a phase shift having a value that is a function of the logic states of the current and future data signals. It is necessary that the phase shift of the phase shifted

clock signal is a function of the logic states of the current and future data signals because the phase comparator (fig. 14, ref. 5301) compares logic states.

Regarding claim.20, Tamura discloses the limitations of claim 1 as applied above. Further, Tamura discloses that the phase shifted clock signal (fig. 14, "clk1") comprises a delay relative to the input clock signal (fig. 14, "clk").

Regarding claim 21, Tamura discloses that a clock synchronization circuit operable to generate a phase shifted clock signal in response to the input clock signal and apply the phase shifted clock signal to clock the respective read data signals out of data drivers as the corresponding output data signals, the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the respective read data and corresponding output data signals as applied to claim 1 above. Additionally, Tamura discloses a plurality of data drivers (fig. 11, refs. 541-543) adapted to receive a respective read data signal (fig. 11, refs. DD1-DDn) and being operable to store the respective read data signal in response to a phase shifted clock signal (fig. 11, refs. clk1-clkn) and output the stored respective read data signal an a corresponding output data signal (fig. 11, outputs of data drivers 541-543). Further, the clock synchronization circuit(s) (fig. 11, refs. 531-533) is adapted to receive an input clock signal (fig. 11, "clk") and respective read and corresponding output data signals. That is, the read data signal is the signal currently being read at time t_0, and the corresponding output data signal was the signal previously read at time t_{0-1}.

Regarding claim 24, Tamura discloses the limitations of claim 21 as applied above. Further, Tamura discloses that the phase shift of the phase shifted clock signal

comprises a phase shift having a value that is a function of the logic states of the current and future data signals. It is necessary that the phase shift of the phase shifted clock signal is a function of the logic states of the current and future data signals because the phase comparator (fig. 14, ref. 5301) compares logic states.

Regarding claim 25, Tamura discloses a data output circuit, comprising: a plurality of data drivers (fig. 11, refs. 541-543), each data driver adapted to receive a respective read data signal (fig. 11, refs. DD1-DDn) and being operable to store the respective read data signal in response to a phase shifted clock signal (fig. 11, refs. clk1-clkn) and output the stored respective read data signal as a corresponding output data signal (fig. 11, outputs of data latches 541-543); a logic circuit (fig. 14, ref. 5301) coupled to receive the respective read data and the corresponding output data signals, and operable to develop a plurality of phase shift control signals (fig. 14, signals input to the delay chains) in response to the respective read data and the corresponding output data signals; and a phase shift circuit (fig. 14, refs. 5302 and 5303) adapted to receive an input clock signal (fig. 14, clk) and coupled to the logic circuit to receive the plurality of phase shift control signals, and operable to generate the phase shifted clock signal (fig. 14, ref. clk1) responsive to the input clock signal, the phase shifted clock signal having a phase shift determined by the plurality of phase shift control signals.

Regarding claim 44, Tamura discloses a method of providing data signals (fig. 11, outputs of data latches 541-543) out of an integrated circuit (col. 1, lines 10-15) in synchronism with a clock signal (fig. 11, "clk") applied to the integrated circuit, the method comprising: detecting a respective first logic state of each data signal (fig. 14,

first state of "DD1"); detecting a respective second logic state of each data signal (fig. 14, second state of "DD1"); determining an output delay from the detected respective first and second logic states (output of phase comparator 5301); and adjusting a delay interval (fig. 14, ref. 5302) relative to a transition of the clock signal based on the determination; and outputting the data signals having the second logic state from the integrated circuit in response to the adjusted delay interval. In the iterative clock synchronization circuit of Tamura, the phase shifting of the input clock signal is related to both the first logic state and the second logic state of each data signal. It is obvious to one having skill in the art that the logic state of data input DD1 is read sequentially. That is, the data inputs have at least first and second logic states. In the method, a "first logic state" was utilized to update the delay in the delay chains 5302 and 5303 of figure 14 via the phase comparator 5301. Subsequently, after the first logic state was latched as the future data signal (output of 540(541)), a second logic state is compared with a clock signal from the delay circuit 5303 delayed according to the "first logic state" to determine an output delay.

Regarding claim 45, Tamura discloses the limitations of claim 44 as applied above. Further, Tamura discloses that the respective first logic state of each data signal comprises a current logic state and wherein the respective second logic state of each data signal comprises an upcoming logic state of the data signal. In the method, a "first logic state" is utilized to update the delay in the delay chains 5302 and 5303 of figure 14 via the phase comparator 5301. Subsequently, the first logic state is latched as the future data signal (output of 540(541)), a second logic state is compared with a clock

signal from the delay circuit 5303 delayed according to the "first logic state" to determine an output delay.

Regarding claim 48, Tamura discloses the limitations of the claim as applied to claim 44 above.

Regarding claim 51, Tamura discloses the limitations of the claim as applied to claims 1 and 44 above.

Regarding claim 57, Tamura discloses the limitations of the claim as applied to claim 44 above.

Regarding claim 58, Tamura discloses the limitations of claim 57 as applied above. Further, Tamura discloses the remaining limitations of claim as applied to claim 45 above.

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura in view of Cox, Jr. et al (US 4019153; hereafter "Cox").

Regarding claim 26, Tamura discloses the limitations of claim 25 as applied above. Tamura disclose a that the logic circuit is a phase detector (fig. 14, ref. 5301) but does not explicitly disclose that the logic circuit comprises a plurality of XNOR gates, each receiving a one of the respective read data and the corresponding output data signals and developing a corresponding one of the plurality of phase shift control signals responsive to the one of the respective read data and corresponding output data signals. However, Cox teaches that a phase detector (fig. 1, ref. 10) can be implemented as a XOR gate (col. 5, lines 60-65) which is well known in the art. One skilled in the art is familiar with the use of XOR gates as phase detectors because they

are effective and extremely easy to implement. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize XOR gates as taught by Cox as the plurality of phase detectors of Tamura because they are effective and the simplest possible implementation of a phase detector. Alternatively, it would have been obvious to one having ordinary skill in the art to utilize XNOR gates depending upon the phases of the signals being compared. For instance, the phase comparators (fig. 14, ref. 5301) of Tamura compare against phase shifted versions of a clock signal clk' which is 180 degrees out of phase with the input clock signal "clk". Therefore, depending upon the specific design, it is obvious that one may wish to utilize XNOR gates rather than XOR gates as phase detectors.

8. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison (US 6173432 – previously cited) in view of Tamura.

Regarding claim 40, Harrison discloses a memory device comprising an address bus (fig. 1, ref. 50; col. 1, line 68, col. 2, lines 20-25); a control bus (fig. 1, ref. 50; col. 2, lines 1-2); a data bus (fig. 1, ref. 130, 132; col. 2, line 64); an address decoder (fig. 1, ref. 82); a read/write circuit coupled to the data bus (fig. 1, refs. 128 and 140); a control circuit coupled to the control bus (fig. 1, ref. 60); a memory cell array coupled to the address decoder, control circuit, and read/write circuit (fig. 1, ref. 80h). Harrison discloses a clock synchronization circuit (fig. 1, ref. 144), but not explicitly as claimed. However, Tamura teaches a clock synchronization circuit as claimed as applied to claim 1 above. Tamura teaches that the clock synchronization circuit is implemented to overcome jitter on the data bus (col. 1). Therefore, it would have been obvious to one

having ordinary skill in the art at the time which the invention was made to replace the clock synchronization and receiver latches (fig. 11, refs. 150) of Harrison with those taught by Tamura because they could advantageously be utilized to reduce jitter due to the high speed of the data transmission.

9. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison in view of Tamura, and in further view of Tsuchida et al (US Pub. 20020078294; hereafter "Tsuchida").

Regarding claim 41, Harrison in view of Tamura disclose the limitations of claim 40 as applied above. Further, Harrison discloses that the memory device may be a SDRAM (col. 1, lines 35-40) but does not explicitly disclose that it is a double data rate SDRAM. However, Tsuchida teaches a double data rate SDRAM (para. 0003) wherein the memory is accessible at both rising and falling edges of the synchronous clock. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a double data rate SDRAM as taught by Tsuchida in place of the SDRAM disclosed by Harrision in view of Tamura because it could advantageously be utilized to provide faster access to the memory.

10. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mastronarde et al (US 6792516; hereafter "Mastronarde") in view of Harrison, and in further view of Tamura.

Regarding claim 42, Mastronarde discloses a computer system according to figure 1, comprising: a data input device (I/O Devices); a data output device (I/O Devices, Display 118); a processor coupled to the data input and output devices (102);

a memory device coupled to the processor (120). Mastronarde discloses that the memory device may be a double data rate SDRAM (col. 2, line 45), but does not disclose all of its claimed features. However, Harrison in view of Tamura teach the remaining claimed features as applied to claim 40 above. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the exemplary memory of Harrison in view of Tamura in place of the memory of Mastronarde because it could advantageously reduce jitter in signals received.

Regarding claim 43, Mastronarde in view of Harrison, and in further view of Tamura disclose the limitations of claim 42 as applied above. Further, Mastronarde discloses that the memory device comprises a DDR SDRAM (col. 2, line 45).

Allowable Subject Matter

11. The indication of allowable subject matter is made regarding claims 63-65.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claims 63-65 are indicated to contain allowable subject matter because the prior art of record does not disclose or obviate the claimed subject matter wherein the respective current and corresponding future logic states are compared directly. That is, the prior art reference Tamura does not disclose that the present data and the data previously latched are directly compared.

13. Claims 2, 3, 5-11, 22, 23, 27-31, 46, 47, 49, 50, 52-56, and 59-62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST. The Applicant is welcomed to contact the Examiner for a discussion regarding the prior art rejections set forth in this office action and any allowable subject matter in the case before a reply is filed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Jason M. Perilla
October 26, 2005

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

jmp